An FPGA-Based Test System for RRAM Technology Characterization

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***Abstract*—Resistive random access memory (RRAM) technologies have recently gained large attention from the academic and industrial research communities. Significant efforts have been made to enhance the performance of the memory stacks from both communities through the design, simulation, and fabrication of novel devices. In this context, improvements can only be confirmed through a thorough device characterization process. Here comes a gap between industry and academia that usually lacks high-end test equipment to perform systematic device characterizations. In this paper, we propose a solution to fill this gap by introducing an easy, affordable, and effective field programmable gate array based RRAM characterization system.**

***Index Terms*—RRAM, technology characterization, FPGA.**

I. Introduction

THE family of solid-state memories has largely expanded during the past decade to identify devices with better density, lower power, more functionality and higher speed in conjunction with a gradual lowering of the cost. Several emerging technologies appeared aiming to go beyond the limitations of the current memory technologies with the ultimate goal of introducing non-volatile features and fast access speed at the same time [1], [2]. In the close future, a crucial role will be played by *Non-Volatile Memories* (NVM). Among them, redox-based *Resistive Random Access Memories* (RRAMs) [3] are considered a good candidate to embody the next-generation technology, due to their very large scalability and good integration in the *Back-End-of-Line* (BEoL) of CMOS process [4].

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Researchers have put many efforts in the last years to enhance RRAM technology, studying new layer stack organization and discovering new properties of the materials to be used as oxide and/or electrodes [5]. Such developments include design, simulation, fabrication and thorough characterization of the proposed devices. In academia, the technology characterization process, together with variability and yield parameters extraction, is mainly performed using manual probe-stations. This solution requires frequent human interaction to be properly set up and fit the needs of the technology under test. A better but more expensive way consists in using semi-automatic probe-stations and test equipments. This kind of approach requires minimal effort by the operator during setup with a substantial initial buying investment that is often not affordable by academic research groups. Moreover, fully-mechanized means of characterization used in the industry world are generally too expensive and process-specific to be used in academia. With the intention of filling this gap, an affordable μ-controller based system has been realized by *Berdan et al.* [6]. With similar objectives, *Kim et al.* [7] realized a CMOS front-end for memory addressing. However, while an ASIC will provide the highest level of performance, modifying the characterization strategy after fabrication can be challenging. On the opposite side, a μ-controller system provides maximum flexibility but lacks of hardware customization / prototyping capabilities.

In this paper, we introduce a low-cost and effective FPGA-based *Memory Characterization System* (MCS). Exploiting a *Field Programmable Gate Array* (FPGA) to implement the characterization strategy, the system will combine both the flexibility of a μ-controller with the hardware customization capabilities of an ASIC. Illustrated in Fig. 1, the MCS includes (i) a *Chip-to-Printed Circuit Board* direct interface through the use of a custom socket; (ii) automatized FPGA-driven measurements; (iii) the possibility of using effective analog on-board current limiting circuits beside the ones provided by external sources. The MCS has been successfully employed to perform sequential electrical tests on RRAM devices fabricated in-house. Full sources of the MCS can be downloaded from [8].

The paper is organized as follows. In Section II, we give a brief background overview about RRAM working principles. In Section III, we focus on the design aspects of the MCS. In Section IV, we show some experimental data gathered using the MCS, showcasing the interest of the MCS approach, while we draw some conclusions in Section V.

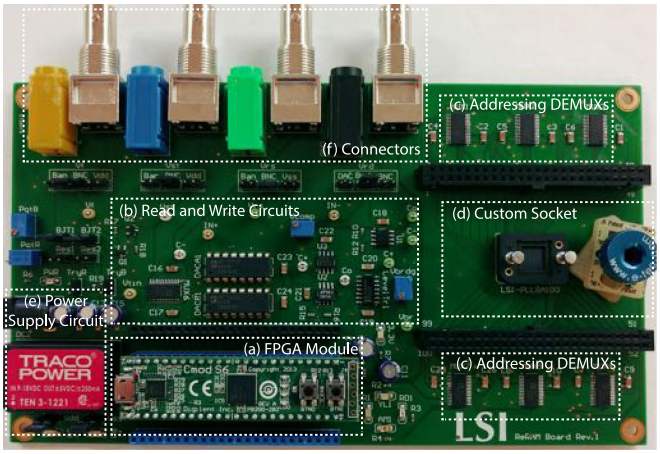

Fig. 1. *Memory Characterization System* (MCS) board including (a) an FPGA module, (b) read and write circuits, (c) addressing demultiplexers, (d) custom socket for the memory chip, (e) power supply circuit and (f) connectors for external equipments.

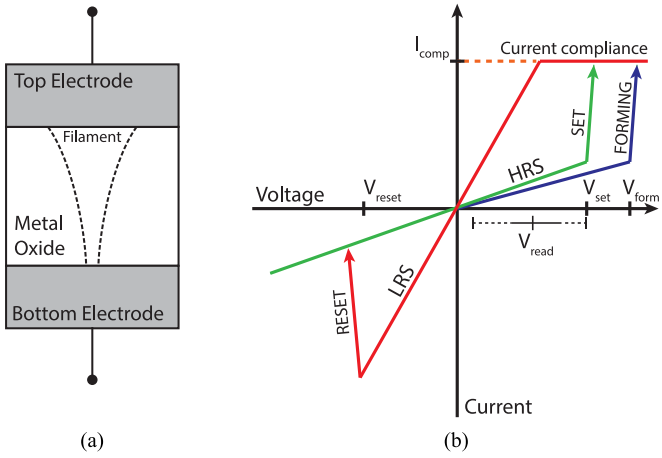

Fig. 2. (a) RRAM layer stack. (b) I-V plot of the switching mechanism.

II. Background

In this section, we introduce the necessary background about RRAM and its electrical control. We also review some prior work focusing on the development of low cost test systems for RRAMs.

A RRAM memory cell is usually consisting of three layers: a metallic *Bottom Electrode* (BE), a switching layer made of one or more transition metal oxides and a metallic *Top Electrode* (TE) as illustrated in Fig. 2(a). Thanks to the switching properties of the oxide stack, the RRAM cell can assume two different resistive states. The transition between the states happens by applying different voltages to the contacts of TE and BE. Fig. 2(b) depicts the I-V plot of the switching mechanism of a RRAM memory. The change of conductivity happens in the oxide layer and is due to the formation (low resistance) and dissolution (high resistance) of a metallic filament [3], [9], [10]. The *set* event (green arrow in Fig. 2(b)) is the transition from *High Resistive State* (HRS) to *Low Resistive State* (LRS). On the other hand, the transition from LRS to HRS, represented by the red arrow, is denoted as *reset*. In order to trigger the resistive switching in fresh pristine samples, i.e., in their initial resistance state, the application of a voltage larger than the *set* voltage is generally necessary. This operation, named *forming* (blue arrow in Fig. 2(b)), is needed only once and activates the memory for the subsequent operation cycles. Note the importance of putting a current compliance to avoid a permanent dielectric breakdown during the *forming* and *set* processes. This is usually achieved by the use of embedded functionalities of semiconductor parameter analyzer, or, more practically, through the access transistor, diode or resistor in series of each memory cell. To read the data from the cell, a small *read* voltage needs to be applied. This has to be lower than the writing threshold, in order not to affect the state of the memory cell, but sufficiently high to have a good sensitivity on the reading result.

Low-cost test systems have been investigated in literature [6], [7]. In [6], a μ-controller based solution is able to perform measurements on a 32×32 crossbar array, previously packaged or interfaced with a probe card. On-board measurements with errors limited to 5% are possible. In [7], a CMOS front-end is used to address a 40×40 memory array co-integrated on top of it. Measurements are taken off-chip with external equipment. In order to combine the flexibility of a μ-controller-based approach with the level of hardware characterization offered by an ASIC, we investigate in this paper an FPGA-based test system.

III. Memory Characterization System

A high-level architecture of the system is provided in Fig. 3(i). The memory represents the central part of the system. Therefore, it is supported by the presence of a controller, in this case an FPGA, that drives the addressing demultiplexers to point to a specific memory cell. The other task of the controller is to select the mode of operation. It is specifically possible to perform four operation on a single cell:

- *Forming*: Initializes a memory cell, that has never been written, in LRS;
- *Reset*: Switches a cell from LRS to HRS;
- *Set*: Switches a cell, that has been previously formed, from HRS to LRS;
- *Read*: Reads the value of the addressed memory cell.

All these operations can be performed sequentially. The read and write functions are fulfilled by the read and write circuits, respectively. In the following, we introduce the different elements of the MCS and their relative functionalities.

A. Addressing Demultiplexers

Without loss of simplicity, addressing is performed by six 16-channel analog demultiplexers, whose inputs are connected to the TE of 96 memory cells of the chip. The specifications on the demultiplexers' resistive paths are stringent: the channel resistance introduced by the MUXs has to be negligible with respect to the access resistance of the chip, that for our case varies from 50 Ω to 250 Ω. Dual supply rail-to-rail operation is required to ensure *set* and *reset* operations occur at opposite polarity. The maximum current allowed per channel has to guarantee a good stability of the device during surge currents due to the *forming*

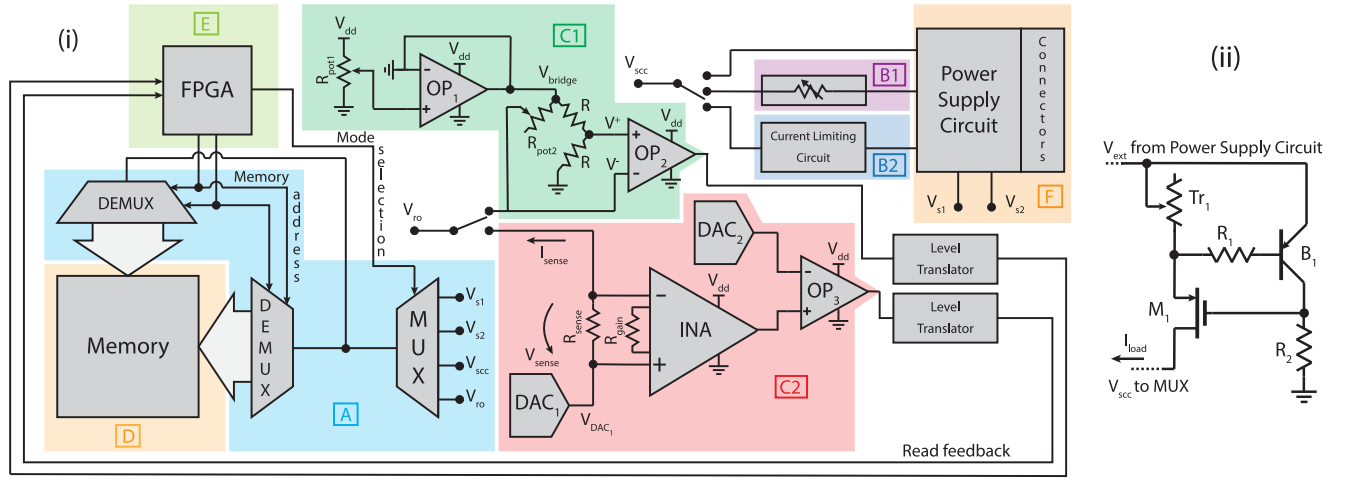

Fig. 3. (i) High-level architecture of the *Memory characterization system* including: (A) Addressing demultiplexers that are in charge of routing signals; Write circuits that limit the current during write operations: (B1) a 5 MΩ trimmer and (B2) an active current limiting circuit; Two read subcircuits to detect the state of the memory cells: (C1) A Wheatstone bridge followed by a comparator, and (C2) two DACs and an INA; (D) A memory die interfaced with a custom socket; (E) An FPGA controller to drive the MUXs and receive the outcomes from the read subcircuits; (F) A power supply circuit providing all the required voltage levels. (ii) Detailed representation of the active current limiting circuit B2.

and *set* processes of the memory. A mode selection multiplexer is also present. It selects and routes the voltage levels required to properly operate the memories during the *forming*, *set*, *reset* and *read* operations. The selection is based on the configuration word controlled by the FPGA. This analog multiplexer fans out into several demultiplexers, that address a specific memory element in the array.

B. Write Circuit

The writing process has to be handled by a specific circuit. In fact, the writing procedure for RRAM memories is complicated due to the various voltage levels needed by each operation to be performed and the current limitation required by the *forming* and *set* operations.

Three different voltage supply lines are available:

- V_{s1}, V_{s2} directly supplied by the power circuit with no voltage or current on-board limitation;
- V_{scc}, provided by the power circuit with the possibility of applying different current compliance methods. All embedded current limiting circuits can be bypassed on this supply line using the *Single-Pole-Triple-Throw* (SPTT) switch shown in Fig. 3(i).

The system has been designed in order to be versatile during *write* operations and proposes two different methods to control RRAMs. That is achieved through independent current limitation circuits that implement the same function using distinct approaches. Fig. 3(i) emphasizes the presence of the two current limiting modes available for V_{scc}:

1) The circuit B1 is consisting of a 5 MΩ trimmer that can be manually adjusted to obtain the desired regime current after the high-to-low resistance switching. The trimmer with resistance R_{B1} is placed in series to the RRAM element with resistance R_{mem}. When a HRS-to-LRS switching happens, R_{mem} transitions from R_{mem}^{HRS} to R_{mem}^{LRS}, where $R_{mem}^{HRS} \gg R_{mem}^{LRS}$. The resulting load current is given by:

$$I_{load} = \frac{V_{prog}}{R_{mem}^{LRS} + R_{B1}} \approx \frac{V_{prog}}{R_{B1}} \text{ when} R_{B1} \gg R_{mem}^{LRS};$$

and is therefore limited by R_{B1}.

2) The circuit B2 is an active current limiting circuit (Fig. 3(ii)). It takes the external voltage V_{ext} from the power circuit. Initially, M_1 is in ohmic conduction mode, passing voltage and current to the memory cell addressed by the MUXs. When an HRS-to-LRS switching event happens, the current through the trimmer Tr_1 exceeds the design limit. As a result, B_1 begins to turn on and modulates the V_{GS} of M_1 in order to limit the load current I_{load}. Since I_{load} is fixed but the memory element has transitioned to a different resistance value, M_1 is pushed in saturation region. R_2 is used to bias M_1 and preserves the negative feedback. The resistor R_1 protects B_1 in the event of a short-circuited load. We chose a MOSFET for M_1 for the lower V_{DS} achievable, limited by its overdrive voltage, when it is in the initial ohmic condition. In this way, I_{load} can be limited simply varying the value of the 200 KΩ trimmer Tr_1:

$$I_{load} \approx \frac{V_{EB}}{R_{Tr_1}};$$

where V_{EB} is the voltage drop between the emitter and base of the BJT.

The active circuit B2 is superior than B1 because the current compliance is independent from the resistance value of the memory under test. However, the simple trimmer-based solution B1 has the advantage of simplicity which is appealing for understanding the basic behavior of the memory during the initial stage of characterization.

Note that, in order to maximize the modularity of the system, external sources can also be used through *Bayonet Neill-Concelman* (BNC) and/or plug connectors in place of the on-board supplies. This allows to have direct access to the

on-chip memories (through the addressing circuit) and use table instrumentation like an external *pulse generator* or a *Source Measurement Unit* (SMU) for higher precision characterization.

C. Read Circuits

Two different read circuits have been implemented (Fig. 3(i)) with the aim of exploring different solutions to read RRAM elements. They can access to the memory block through a jumper that allows mutually-exclusive selection of the two methods. The jumper function is represented with a *Single-Pole-Double-Throw* (SPDT) switch in Fig. 3(i). The path to the memory is then determined by the addressing demultiplexers, controlled by the FPGA:

1) The circuit C1 is based on a Wheatstone bridge. It is used to discriminate between the two resistive states that a RRAM cell can assume. R_{pot1} is used to adjust the supply voltage V_{bridge} buffered on top of the bridge by OP_1. The voltage drop on the memory element depends on the value of the resistance R_{pot2} in series with it and the supply voltage V_{bridge}. To limit any disturbance during a *read* operation (e.g., unwanted switching event), the supply voltage should be lower than the *set* voltage (that is a technological parameter of the memory element). That is because the value of R_{pot2} can be potentially set to $0\,\Omega$ and the memory element would have all the read voltage on its terminals. Consequently, R_{pot2} has to be regulated in such a way that the negative pin $(-)$ of OP_2 moves around the threshold on the positive pin $(+)$, as the memory element switches:

$$V^{-}_{\text{LRS}} \; < \; V^{+} \; < \; V^{-}_{\text{HRS}};$$

where:

$$V^{-}_{\text{LRS}} = V_{\text{bridge}} \frac{R^{\text{LRS}}_{\text{mem}}}{R_{\text{pot2}} + R^{\text{LRS}}_{\text{mem}}};$$

$$V^{-}_{\text{HRS}} = V_{\text{bridge}} \frac{R^{\text{HRS}}_{\text{mem}}}{R_{\text{pot2}} + R^{\text{HRS}}_{\text{mem}}};$$

$$V^{+} = V_{\text{bridge}} \frac{R}{R+R} = \frac{V_{\text{bridge}}}{2}.$$

The comparator OP_2 will then present a high output (5 V) or low output (0 V) if the cell is in LRS or HRS, respectively.

2) The circuit C2 is a current sense circuit. The digital-to-analog converter DAC_1 generates the read voltage V_{DAC_1} to bias and sense the memory during a *read* operation. It is controlled by the FPGA to obtain an output voltage range from 0 V to 2.56 V with 6-bit precision. By measuring the voltage drop V_{sense} on the sense resistor R_{sense}, we can infer the actual state of the RRAM cell:

$$I_{\text{sense}} = \frac{V_{DAC_1}}{R_{\text{mem}} + R_{\text{sense}}} \approx \frac{V_{DAC_1}}{R_{\text{mem}}} \text{ when } \text{R}_{\text{sense}} \ll \text{R}_{\text{mem}};$$

$$V_{\text{sense}} = I_{\text{sense}} R_{\text{sense}}.$$

The signal V_{sense} is amplified by the *INstrumentation Amplifier* (INA) and compared by OP_3 to a threshold, generated by DAC_2 and empirically determined in relation to the RRAM properties.

The outputs of the two circuits go to the level translators that adjust the dynamic range to the logic levels of the FPGA controller.

D. Custom Socket

In order to have a direct *Chip-to-Printed Circuit Board* interface, we designed a custom socket that can hold a die, right after its fabrication. The custom socket is directly fastened to the PCB and ensures the connection with the chip through the use of spring contacts. For that, a standardized format for the test-chip pinout has been defined, and is available in [8]. The die is placed in a *flip chip* configuration. This technique ensures the die in firm position and full contact with the PCB that hosts the whole system.

IV. Experimental Results

In this section, we discuss the realization of the MCS and give a brief description of the fabrication process flow of the memory under test. We then showcase the flexibility of the MCS through three possible applications: an automated time characterization, a variability and yield test and a demonstration of read/write operations in standalone mode.

A. MCS Realization

The MCS has been realized on a PCB as shown in Fig. 1. *Analog Devices ADG1606* are used as addressing and mode selection multiplexers; The PNP bipolar transistor and the PMOS in the current limiting circuit are implemented as discrete components on the PCB. B_1 is a *Fairchild MMBT5087* model while *NXP BSS84* has been used for M_1. All the operational amplifiers are *Analog Devices AD8616*. For the instrumentation amplifier in the read circuit, we used a *Linear Technology LT1167* while the voltage level translator is a *Texas Instruments TXS0104ED*. All DACs are Analog Devices AD558.

B. Memory Under Test

The MCS was used to test a RRAM chip fabricated in-house. The considered $\text{Pt/HfO}_2\text{/Ti/Pt}$ stack was obtained as follows:

- Pt layer of 100 nm deposited by DC sputtering;
- HfO_2 layer of 10 nm deposited through *Atomic Layer Deposition* (ALD);
- Ti layer of 10 nm and Pt layer of 100 nm deposited by DC sputtering technique.

The memory chip contains 96 individual 1R memory cells sharing a common BE terminal. Full test-chip layout can be found in the MCS documentation [8] and is reported in Fig. 4. The bottom electrode line (in green) forms a ring around the test-chip and all individual 96 RRAMs are formed by individual top electrode lines (in red) that cross the bottom electrode ring. The electrical properties of the memory stack have the following mean values: $V_{\text{form}} = 2$ V, $V_{\text{set}} = 2$ V, $V_{\text{reset}} = -1.2$ V, $I_{\text{comp}} = 700\ \mu$A, LRS $= 1\ \text{k}\Omega$, HRS $= 30\ \text{k}\Omega$. A study about this process technology and its post-fabrication aging degradation can be found at [11].

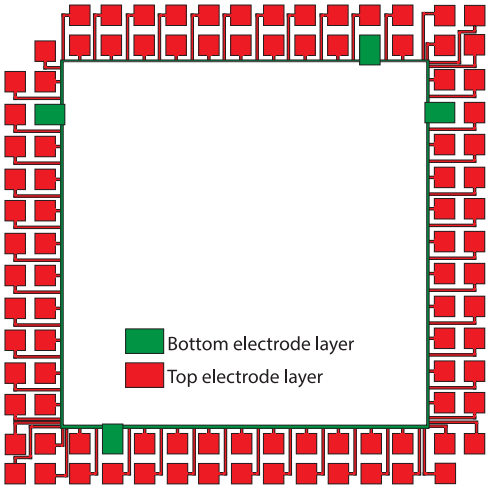

Fig. 4. Test-chip layout organization. Complete layout sources can be found in the attached documentation [8].

C. MCS Application 1: Automated Time Characterization

The MCS is used to perform automated time characterization of multiple devices in sequence. We applied a sample measurement sequence to a chip fabricated using the technology process flow mentioned above. A NI PXIe-4141 SMU has been used as external measurement equipment directly coupled with MCS. Measurements are resulting from the same voltage sequence of 5 s applied sequentially by the SMU on 3 different devices of the same chip. The test sequence is composed of 5 sequential operations, *read-forming-read-reset-read* of 0.5 s duration each. Every operation is followed by a pause, namely a no-operation, of 0.5 s. *Read* operation is performed with a square pulse of 0.2 V amplitude. *Forming* (*reset*) were performed using a voltage sawtooth function with a wave period of 0.5 s, an amplitude of 5 V (-2 V) and a slew-rate of 10 Vs^{-1} (-4 Vs^{-1}) respectively. A current compliance of 800 μA has been used during *forming* operations using the SMU embedded functionalities. Since measurements have been performed applying voltage test waveforms that are slowly-varying with maximum sampling time down to 20 ms, the characterization has been performed in quasi-static conditions. Therefore, on-board and off-board connections have negligible impact on the accuracy of the system and follow their ideal short-circuit model. Addressing and Mode Selection MUXs, interposed between the SMU and the memory element under test, exhibit a total typical series resistance of 9 Ω. This constant measurement offset can eventually be subtracted during post-treatment in order to improve precision. Besides this offset, the accuracy of the gathered data is solely given by the SMU. No other series resistance is interposed between the memory under test and the measurement system. Exact voltage/current/resistance levels shown in Fig. 5 are collected by the SMU. The three devices have been successfully formed in LRS and reset back into HRS. Note that device 2 presents a much larger HRS/LRS resistance ratio compared to the other devices that can be attributed to process variations. The aim of this paper is to discuss the MCS, as an easy way to characterize such data and facilitate research. Commenting the reasons of this variability is out of the scope of this paper.

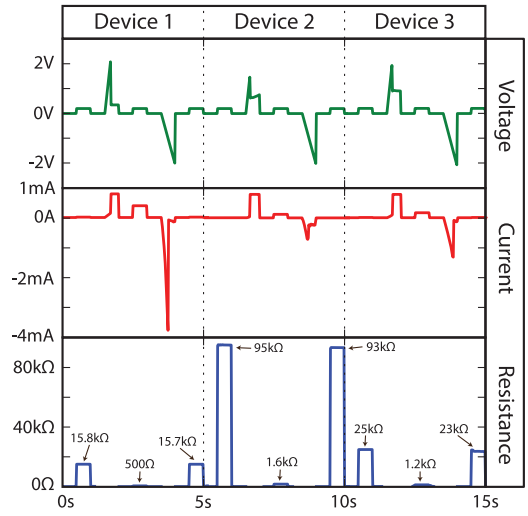

Fig. 5. Extracted portion of the time characterization sequences of three adjacent RRAM cells (Dev1 - DEMUX 1 / OUTPUT 9, Dev2 - DEMUX 2 / OUTPUT 14, Dev3 - DEMUX 5 / OUTPUT 4; naming conventions for MUXs and their connections can be found in the attached documentation [8]).

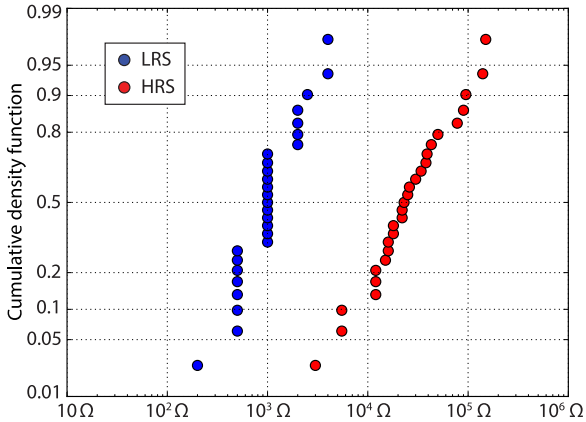

Fig. 6. Normal probability plot of LRS and HRS of 27 cells on the same chip.

D. MCS Application 2: Variability and Yield Testing

The MCS is also used to gather automated statistical data from the memory chip. Using the same setup as before, we acquired data about the higher HRS and lower LRS reached by 27 memory cells of the same chip. Fig. 6 shows a normal probability plot of the results. This chart gives an idea about the variability and yield that a specific technology can reach after the fabrication process.

E. MCS Application 3: Standalone Read/Write Operations With On-Board Current Limitation

Finally, we used the MCS in standalone mode during write and read procedures using its on-board current limitation functionalities. The NI PXIe-4141 SMU has been used for applying voltage waveforms and measuring precise voltage, current, resistance on devices. We performed the experiment using only square wave pulses in order to emulate digital signals applied

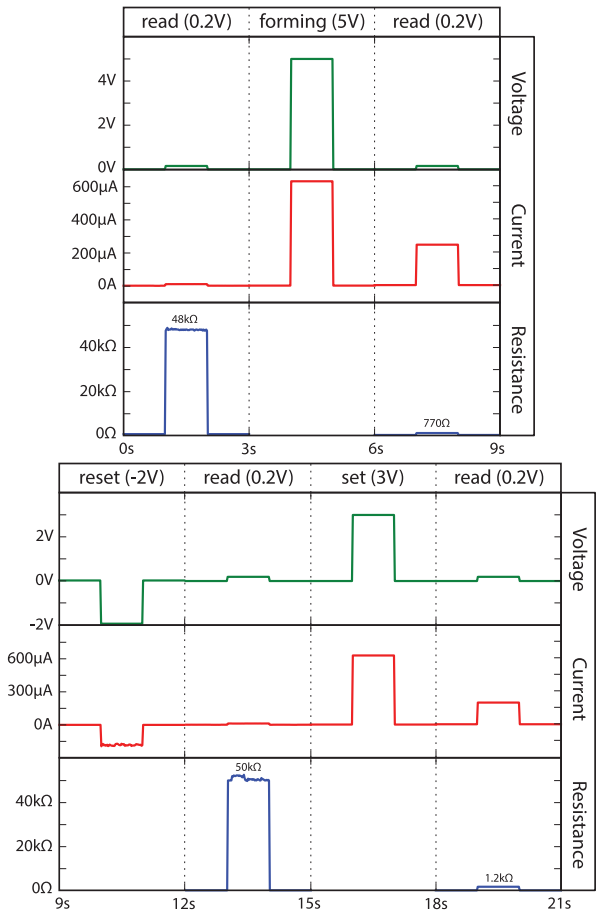

Fig. 7. Measured values of a *read-forming-read-reset-read-set-read* sequence on a memory cell, using the active current limiting circuit during *forming* and *set* operations. The device is selected using DEMUX 1 / OUTPUT 12. Naming conventions for MUXs and their connections can be found in the attached documentation [8].

to the memories. The sequence consists of *read-forming-read-reset-read-set-read* operations of 1s duration each, as in Fig. 7. During the *forming* and *set* operations, we apply a square pulse of 5 V and 3 V respectively, to the V_{ext} rail of the active current limiting circuit (Fig. 7) using an external connector and the V_{scc} line is selected by the Mode Selection MUX (Fig. 3(i)). Therefore, the current compliance is not applied using SMU functionalities and the *forming/set* procedure is performed using circuit B2. The compliance level is set by adjusting the value of the trimmer Tr_1 as discussed in Section III-B. During the *forming/set* operation, the discrete BJT B_1 is biased with a current $I_{\text{E}} \approx 10\ \mu\text{A}$ by the negative feedback loop. The BJT V_{BE}-I_{E} characterization data shows $V_{\text{EB}} \approx 0.55$ V in that bias condition. Setting the trimmer to 860 Ω, we obtain a current compliance of:

$$I_{\text{load}} \approx \frac{V_{\text{EB}}}{R_{Tr_1}} \approx \frac{0.55\ \text{V}}{860\ \Omega} \approx 640\,\mu\text{A}.$$

During *reset* and *read* operations, the FPGA selects the supplementary line V_{s1} using the Mode Selection MUX, in order to bypass the current limiting circuit. *Reset* and *read* pulses have respectively −2 V and 0.2 V amplitude. Exact voltage/current/resistance levels are collected by the SMU, directly connected to the V_{s1} line, with no introduced offsets. No current compliance is applied during these operations.

V. Conclusion

We have shown a realization of an FPGA-based system able to perform easy memory characterization with a *Chip-to-Printed Circuit Board* direct interface, automatized measurements driven by an FPGA controller and current compliance carried out by specific on-board circuits. This system brings many advantages: modularity in the measurement method chosen that can be external or internal; easy access to the die just after fabrication; multiple methods of limiting the current during *forming* and *set* processes.

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